In the Claims:

Claim 1 (previously presented): A one time programmable solid-state device comprising:

a programmable memory unit embedded in a die within the one time programmable solid-state device;

a driver circuit that programs the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations; and

an access circuit that enables access to the programmable memory unit, wherein the access circuit is configured to drive a row of the memory cells to ground that are to be read out.

Claim 2 (previously presented): The one time programmable solid-state device of claim 1 wherein the programmable memory unit includes a number of memory cells having a gate.

Claim 3 (original): The one time programmable solid-state device of claim 2 wherein the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells.

Claim 4 (original): The one time programmable solid-state device of claim 3 wherein the

number of rows of memory cells is equal to a predetermined number, and the number of columns of memory cells is equal to the predetermined number.

Claim 5 (original): The one time programmable solid-state device of claim 2 wherein each memory cell in the number of memory cells is a capacitor.

Claim 6 (original): The one time programmable solid-state device of claim 2 wherein each memory cell in the number of memory cells is a transistor.

Claim 7 (original): The one time programmable solid-state device of claim 6 wherein the transistor is a field-effect transistor (FET).

Claim 8 (previously presented): The one time programmable solid-state device of claim 2 wherein a code is stored in the programmable memory unit.

Claim 9 (original): The one time programmable solid-state device of claim 8 wherein the code is a serial number.

Claim 10 (original): The one time programmable solid-state device of claim 8 wherein the code is a product identifier.

Claim 11 (original): The one time programmable solid-state device of claim 2 wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one

predetermined configuration value in the programmable memory unit.

Claim 12 (original): The one time programmable solid-state device of claim 2 wherein the number of memory cells contains an address of at least one defective pixel that is located in an imaging device on the die of the one time programmable solid-state device.

Claim 13 (original): The one time programmable solid-state device of claim 12 wherein at least one memory cell of the number of memory cells is permanently encoded.

Claim 14 (original): The one time programmable solid-state device of claim 13 wherein the at least one memory storage cell is permanently encoded by application of an effective voltage to the gate at least equal to a breakdown voltage of a gate oxide on the surface of the gate.

Claim 15 (original): The one time programmable solid-state device of claim 1 wherein the driver circuit and access circuit are embedded in the die.

Claim 16 (previously presented): The one time programmable solid-state device of claim 15 wherein the programmable memory unit includes a number of memory cells having a gate.

Claim 17 (original): The one time programmable solid-state device of claim 16 wherein

the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells.

Claim 18 (original): The one time programmable solid-state device of claim 17 wherein the number of rows of memory cells is equal to a predetermined number, and the number columns of memory cells is equal to the predetermined number.

Claim 19 (original): The one time programmable solid-state device of claim 16 wherein each memory cell in the number of memory cells is a capacitor.

Claim 20 (original): The one time programmable solid-state device of claim 16 wherein each memory cell in the number of memory cells is a transistor.

Claim 21 (original): The one time programmable solid-state device of claim 20 wherein the transistor is a field-effect transistor (FET).

Claim 22 (previously presented): The one time programmable solid-state device of claim 16 wherein a code is stored in the programmable memory unit.

Claim 23 (original): The one time programmable solid-state device of claim 22 wherein the code is a serial number.

Claim 24 (original): The one time programmable solid-state device of claim 22 wherein

the code is a product identifier.

Claim 25 (original): The one time programmable solid-state device of claim 16 wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit.

Claim 26 (original): The one time programmable solid-state device of claim 16 wherein the number of memory cells contains an address of at least one defective pixel that is located in an imaging device on the die of the one time programmable solid-state device.

Claim 27 (original): The one time programmable solid-state device of claim 26 wherein at least one memory cell of the number of memory cells is permanently encoded.

Claim 28 (original): The one time programmable solid-state device of claim 27 wherein the at least one memory storage cell is permanently encoded by application of an effective voltage to the gate at least equal to a breakdown voltage of a gate oxide on the surface of the gate.

Claim 29 (previously presented): A method for programming a one time programmable solid-state device comprising:

writing, with a driver circuit, to a programmable memory unit embedded in a die within the programmable solid-state device locations of defective pixels by programming

memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations; and

accessing, with an access circuit, the one time programmable solid-state device, wherein the access circuit drives a row of the memory cells to ground that are to be read out.

Claim 30 (original): The method of claim 29 wherein the programmable solid-state device is a solid-state imaging device.

Claim 31 (previously presented): The method of claim 30 further including identifying a defective pixel within the solid-state imaging device.

Claim 32 (original): The method of claim 29 wherein the driver circuit and access circuit are embedded in the die.

Claim 33 (previously presented): The method of claim 32 wherein the programmable solid-state device is a solid-state imaging device.

Claim 34 (original): The method of claim 29 wherein writing further includes storing a code in the programmable memory unit.

Claim 35 (original): The method of claim 34 wherein the code is a serial number.

Claim 36 (original): The method of claim 34 wherein the code is a product identifier.

Claim 37 (previously presented): A method of data storage comprising:

identifying an address of a defective pixel in a photosensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device;

storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations; and

driving a row of the memory cells to ground that are to be read out.

Claim 38 (original): The method of claim 37 wherein identifying includes identifying a row and a column that corresponds to the defective pixel in the photosensor.

Claim 39 (original): The method of claim 38 wherein storing includes permanently encoding the address of the defective pixel in the programmable memory unit.

Claim 40 (original): The method of claim 39 wherein storing further includes permanently encoding the address into a row having a plurality of transistors in the

programmable memory unit, where each transistor in the plurality of transistors has a gate.

Claim 41 (original): The method of claim 40 wherein storing further includes breaking down the gate on each transistor in the plurality of transistors that corresponds to a logic 1 in the address.

Claim 42 (previously presented): The method of claim 41 further including accessing the address stored in the programmable memory unit.

Claim 43 (original): The method of claim 42 wherein accessing further includes detecting a leakage current flowing through the gate oxide of at least one of the transistors.

Claim 44 (original): The method of claim 43 wherein accessing further includes amplifying the detected leakage current.

Claim 45 (previously presented): A one time programmable solid-state device comprising:

a programmable memory unit embedded in a die within the one time programmable solid-state device;

means for programming the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the

corresponding location, and wherein the individual memory cells are associated with respective pixel locations; and

means for enabling access to the programmable memory unit, wherein the means for enabling access is configured to drive a row of the memory cells to ground that are to be read out.

Claim 46 (previously presented): The one time programmable solid-state device of claim 45 wherein the programmable memory unit includes a number of memory cells having a gate.

Claim 47 (original): The one time programmable solid-state device of claim 46 wherein the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells.

Claim 48 (original): The one time programmable solid-state device of claim 47 wherein the number of rows of memory cells is equal to a predetermined number, and the number columns of memory cells is equal to the predetermined number.

Claim 49 (original): The one time programmable solid-state device of claim 46 wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit.

Claim 50 (original): The one time programmable solid-state device of claim 45 wherein

the programming means and access enabling means are embedded in the die.

Claim 51 (previously presented): A one time programmable solid-state device comprising:

means for writing to a programmable memory unit embedded in a die within the programmable solid-state device locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations; and

means for accessing the one time programmable solid-state device, wherein the means for accessing is configured to drive a row of the memory cells to ground that are to be read out.

Claim 52 (original): The one time programmable solid-state device of claim 51 wherein the programmable solid-state device is a solid-state imaging device.

Claim 53 (original): The one time programmable solid-state device of claim 51 wherein the writing means further includes means for storing a code in the programmable memory unit.

Claim 54 (original): The one time programmable solid-state device of claim 53 wherein the code is a serial number.

Claim 55 (original): The one time programmable solid-state device of claim 53 wherein

the code is a product identifier.

Claim 56 (original): The one time programmable solid-state device of claim 51 wherein the writing means and accessing means are embedded in the die.

Claim 57 (previously presented): A one time programmable solid-state device comprising:

means for identifying an address of a defective pixel in a photosensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device; and

means for storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device, wherein the means for storing is configured to drive a row of memory cells in the two-dimensional array to ground that are to be read out.

Claim 58 (original): The one time programmable solid-state device of claim 57 wherein the identifying means includes means for identifying a row and a column that corresponds to the defective pixel in the photosensor.

Claim 59 (original): The one time programmable solid-state device of claim 58 wherein the storing means includes means for permanently encoding the address of the defective pixel in the programmable memory unit.

Claim 60 (previously presented): The one time programmable solid-state device of

claim 1 wherein the driver circuit is configured to drive an inverter to ground corresponding to a row of the memory cells that are to be programmed.

Claim 61 (previously presented): The method of claim 29, the method further comprising driving, with the driver circuit, an inverter to ground corresponding to a row of the memory cells that are to be programmed.

Claim 62 (previously presented): The method of claim 37, the method further comprising driving an inverter to ground corresponding to a row of the memory cells that are to be programmed.

Claim 63 (previously presented): The one time programmable solid-state device of claim 45 wherein the means for programming is configured to drive an inverter to ground corresponding to a row of the memory cells that are to be programmed.

Claim 64 (previously presented): The one time programmable solid-state device of claim 51 wherein the means for writing is configured to drive an inverter to ground corresponding to a row of the memory cells that are to be programmed.

Claim 65 (previously presented): The one time programmable solid-state device of claim 57, the device further comprising means for driving configured to program the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein

the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations.